

**WHAT IS CLAIMED IS:**

1. For use in a wide-issue pipelined processor, a mechanism  
for reducing pipeline stalls between conditional branches,  
comprising:

a mispredict program counter (PC) generator that generates a  
mispredict PC value for each conditional branch instruction in a  
pipeline of said processor; and

mispredict PC storage, coupled to said mispredict PC  
generator, that stores said mispredict PC value at least until a  
resolution of said conditional branch instruction occurs and makes  
said mispredict PC value available to a PC of said processor if  
said resolution results in a mispredict condition.

2. The mechanism as recited in Claim 1 wherein said  
mispredict PC generator is associated with a static branch  
predictor of said processor.

3. The mechanism as recited in Claim 1 wherein said  
mispredict PC generator generates a branch prediction and said  
mispredict PC value in a single clock cycle.

4. The mechanism as recited in Claim 3 wherein said branch  
prediction is employed to prefetch instructions.

5. The mechanism as recited in Claim 1 wherein a mispredict  
2 PC queue of said mispredict PC storage has at least as many slots  
3 as said pipeline has stages.

6. The mechanism as recited in Claim 1 wherein said  
2 mispredict PC value moves through registers of said mispredict PC  
3 storage as said conditional branch instruction moves through stages  
4 in said pipeline.

7. The mechanism as recited in Claim 1 wherein said  
2 resolution occurs in an execution stage of said pipeline.

8. The mechanism as recited in Claim 1 wherein said  
2 processor is a digital signal processor.

1 9. For use in a wide-issue pipelined processor, a method of  
2 reducing pipeline stalls between conditional branches, comprising:  
3 generating a mispredict program counter (PC) value for each  
4 conditional branch instruction in a pipeline of said processor; and  
5 storing said mispredict PC value at least until a resolution  
6 of said conditional branch instruction occurs; and  
7 making said mispredict PC value available to a PC of said  
8 processor if said resolution results in a mispredict condition.

1 10. The method as recited in Claim 9 wherein said mispredict  
2 PC generator is associated with a static branch predictor of said  
3 processor.

1 11. The method as recited in Claim 9 wherein said generating  
2 is carried out in a single clock cycle, said method further  
3 comprising generating a branch prediction in a single clock cycle.

1 12. The method as recited in Claim 11 further comprising  
2 employing said branch prediction to prefetch instructions.

1 13. The method as recited in Claim 9 wherein a mispredict PC  
2 queue of said mispredict PC storage has at least as many slots as  
3 said pipeline has stages.

14. The method as recited in Claim 9 further comprising  
2 moving said mispredict PC value through registers in said  
3 mispredict PC storage as said conditional branch instruction moves  
4 through stages in said pipeline.

15. The method as recited in Claim 9 wherein said resolution  
2 occurs in an execution stage of said pipeline.

16. The method as recited in Claim 9 wherein said processor  
2 is a digital signal processor.

17. A digital signal processor, comprising:

a pipeline having stages capable of executing conditional branch instructions;

a wide-issue instruction issue unit;

a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in said pipeline; and

mispredict PC storage, coupled to said mispredict PC generator, that stores said mispredict PC value at least until a resolution of said conditional branch instruction occurs and makes said mispredict PC value available to a PC of said DSP if said resolution results in a mispredict condition.

18. The DSP as recited in Claim 17 wherein said mispredict PC generator is associated with a static branch predictor in said instruction issue unit.

19. The DSP as recited in Claim 17 wherein said mispredict PC generator generates a branch prediction and said mispredict PC value in a single clock cycle.

20. The DSP as recited in Claim 19 wherein said branch prediction is employed to prefetch instructions.

21. The DSP as recited in Claim 17 wherein a mispredict PC  
2 queue of said mispredict PC storage has at least as many slots as  
3 said pipeline has said stages.

22. The DSP as recited in Claim 17 wherein said mispredict PC  
2 value moves through registers in said mispredict PC storage as said  
3 conditional branch instruction moves through said stages.

23. The DSP as recited in Claim 17 wherein said resolution  
2 occurs in an execution stage of said pipeline.